2814 #51/2
6/25/03 Mellin

Docket No.: MAS-FIN-193

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By: _____ Date: 4/5/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Harry Hedler et al.
Applic. No.	:	10/022,226
Filed	:	December 17, 2001
Title	:	Electronic Component with Flexible Bonding Pads and Method of Producing Such a Component
Art Unit	:	2814

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 4,001,870 (Saiki et al.), dated January 4, 1977;

United States Patent No. 4,074,342 (Honn et al.), dated February 14, 1978;

United States Patent No. 4,365,264 (Mukai et al.), dated December 21, 1982;

United States Patent No. 4,618,878 (Aoyama et al.), dated October 21, 1986;

United States Patent No. 4,813,129 (Karnezos), dated March 21, 1989;

United States Patent No. 4,885,126 (Polonio), dated December 5, 1989;

United States Patent No. 4,902, 606 (Patraw), dated February 20, 1990;

United States Patent No. 5,072,520 (Nelson), dated December 17, 1991;

United States Patent No. 5,148,265 (Khandros et al.), dated September 15, 1992;

United States Patent No. 5,148,266 (Khandros et al.), dated September 15, 1992;

United States Patent No. 5,180,311 (Schreiber et al.), dated January 19, 1993;

United States Patent No. 5,420,329 (Zeiss), dated May 30, 1995;

United States Patent No. 5,455,390 (DiStefano et al.), dated October 3, 1995;

United States Patent No. 5,477,087 (Kawakita et al.), dated December 19, 1995;

United States Patent No. 5,489,749 (DiStefano et al.), dated February 6, 1996;

United States Patent No. 5,491,302 (DiStefano et al.), dated February 13, 1996;

United States Patent No. 5,604,380 (Nishimura et al.), dated February 18, 1997;

United States Patent No. 5,619,017 (DiStefano et al.), dated April 8, 1997;

United States Patent No. 5,666,270 (Matsuda et al.), dated September 9, 1997;

United States Patent No. 5,679,977 (Khandros et al.), dated October 21, 1997;

United States Patent No. 5,749,997 (Tang et al.), dated May 12, 1998;

United States Patent No. 5,777,379 (Karavakis et al.), dated July 7, 1998;

United States Patent No. 5,874,782 (Palagonia), dated February 23, 1999;

United States Patent No. 5,907,785 (Palagonia), dated May 25, 1999;

United States Patent No. 6,284,563 B1 (Fjelstad), dated September 4, 2001;

Anonymous: "Method of Testing Chips and Joining Chips to Substrates", XP-000169195.

Respectfully submitted,

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